

FIG. 1

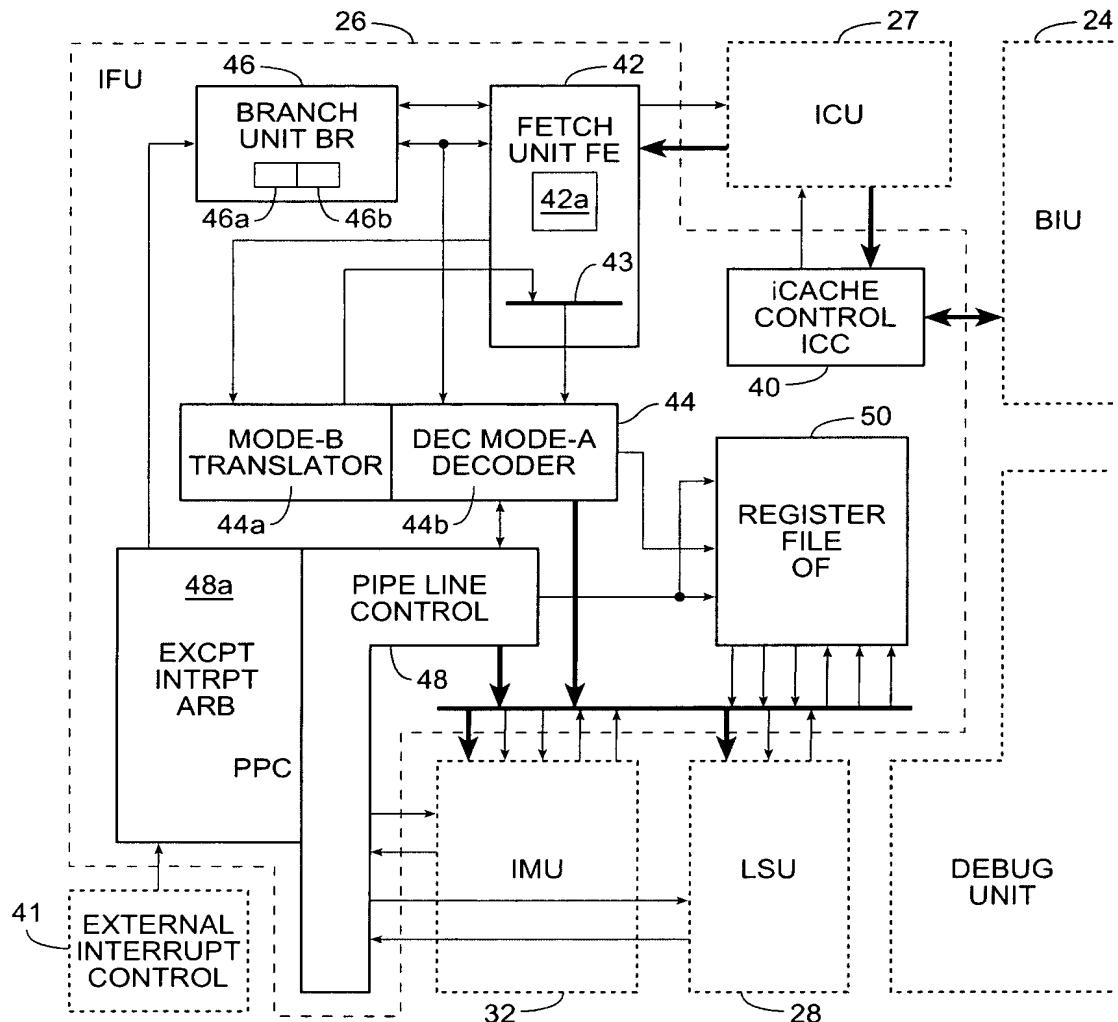


FIG. 2

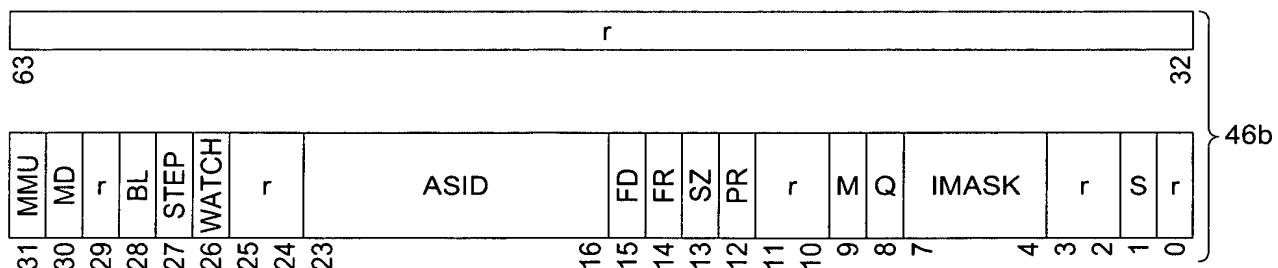


FIG. 3

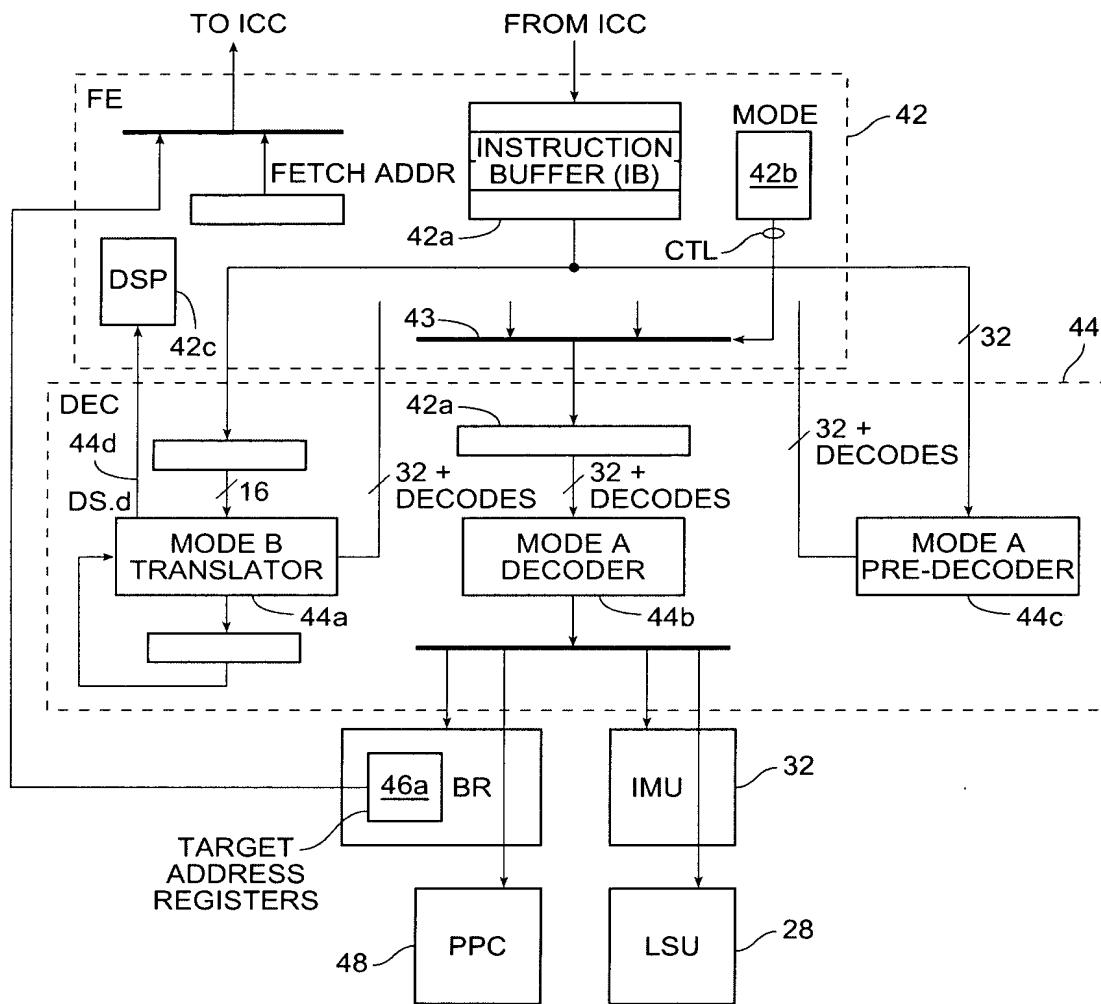


FIG. 4

MODE B STATE	DESCRIPTION	MODE A STATE
PC	Program counter	Lower 32 bits of PC
R <sub>i</sub> where i is in [0,15]	Mode B general-purpose registers	lower 32 bits of R <sub>i</sub> where i is in [0,15]
PR	Procedure link register	Lower 32 bits of R <sub>18</sub>
GBR	Global base register	Lower 32 bits of R <sub>27</sub>
MACL	Multiply-accumulate low	Lower 32 bits of R <sub>24</sub>
MACH	Multiply-accumulate high	Upper 32 bits of R <sub>24</sub>
T	Condition code flag	Bit 0 of R <sub>25</sub>
S	Multiply-accumulate saturation flag	SR.S
M	Divide-step M flag	SR.M
Q	Divide-step Q flag	SR.Q

FIG. 5

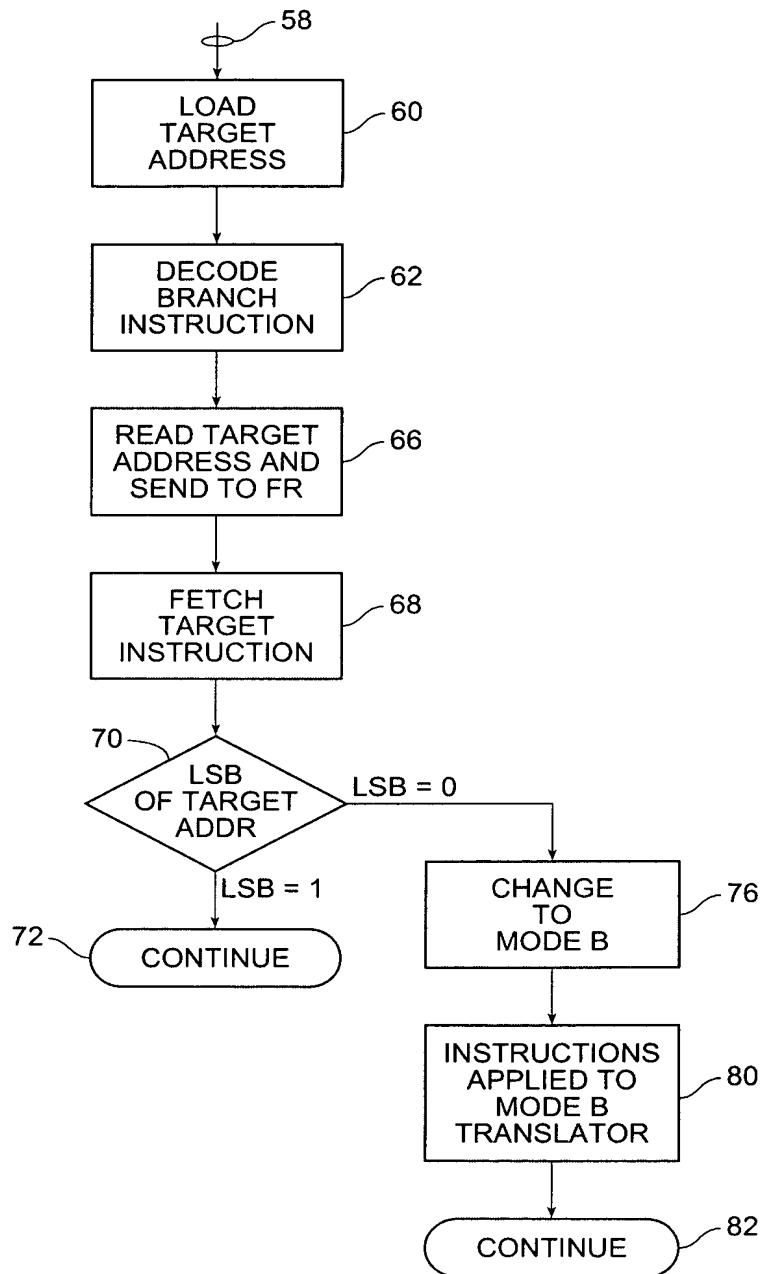


FIG. 6